# MONOLITHIC FRONT-END IC'S FOR INTERPOLATING CATHODE PAD AND STRIP DETECTORS FOR GEM

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**ABSTRACT**

We are developing CMOS circuits for readout of interpolating cathode strip and pad chambers for the GEM experiment at the SSC. Because these detectors require position resolution of about 1% of the strip pitch, the electronic noise level must be less than 2000 electrons.

Several test chips have been fabricated to demonstrate the feasibility of achieving the combination of low noise, speed, and wide dynamic range in CMOS. Results to date show satisfactory noise and linearity performance. Future development will concentrate on radiation-hardening the central tracker ASIC design, optimizing the shaper peaking time and noise contribution, providing more user-configurable output options, and packaging and test issues.

## I. Introduction

In multiwire gas proportional chambers with interpolating cathode readout a position coordinate measurement is obtained by determining the center-of-gravity of the charge distribution induced on a segmented pad or strip cathode. By orienting the strips at right angles to the anode wires, the mean position of the charge distribution can vary in a continuous way, permitting a precise determination of the particle's position of incidence. For example, with a cathode strip pitch of 5 mm and a signal-to-noise ratio of order 100:1, position resolutions in the range 50 - 100 μm are obtainable.

These detectors are well suited for charged-particle tracking at the SSC because:

- position resolution of a fraction of the channel-to-channel spacing can be achieved by interpolation

- they can cover large areas at low cost

- they can be designed to have a fast ( ~ 30 nsec) charge collection time, permitting unambiguous bunch crossing assignment and output to triggers

- they can be easily constructed of radiation-hard materials.

In GEM, interpolating cathode pad chambers (IPC) and cathode strip chambers (CSC) have been chosen for the outer central tracker and muon systems, respectively. Because of the enormous channel counts (0.4 and $2 \times 10^6$ respectively), a monolithic approach to the front-end electronics is essential. It is also important to minimize the number of off-chip components, and to incorporate calibration and test capabilities into the chip.

Figure 1 shows the tracker IPC and muon CSC front end electronics block diagrams. In the CSC architecture, the front end ASIC must provide fast timing outputs, and a track-and-hold and analog multiplexer for the amplitude readout. In contrast, the IPC front end ASIC consists simply of a preamp and shaper.

The design requirements for the IPC and CSC are shown in Table I. Because the chamber construction and operating conditions are similar, the input signal charge and gain requirement is comparable for both applications. This noise requirements are also similar, since the desired interpolation accuracy is about the same. The CSC chambers have larger strips and experience a much lower rate than the IPCs, therefore their capacitance is 3-5 times higher and pulse shaping times can be longer. Finally, the IPC electronics must withstand a high radiation environment.

## II. Noise optimization

Although bipolar, JFET, GaAs MESFET, and MOS devices could be used for the preamplifier, we chose CMOS because of its low cost, widespread availability, CAD support, and ability to incorporate switching functions. The input device must be designed to minimize noise by selecting the device polarity, dimensions, and bias conditions, as well as by careful layout to minimize parasitic gate and substrate resistances. Using the data in Table I, we find that the equivalent input noise voltage density must be les than 0.5 and 0.9 nV/√Hz, respectively, for the IPC and CSC (averaged over the bandwidth). This may be expressed as an equivalent input noise resistance of 15 and 50 Ω, respectively. The average noise current spectral density (parallel noise) must be less than 1.3 (IPC) and 0.23 (CSC) pA/√Hz.

The peaking time for the IPC (30 nsec) falls in a range where channel thermal noise dominates, while the CSC (300-500 nsec) is above the 1/f noise corner time constant. Therefore we chose to use a PMOS input device, whose 1/f noise is 3-10 times smaller than NMOS, for the CSC front end. For the IPC, channel thermal noise is dominant and NMOS is more power efficient.

We used Orbit Semiconductor's 2 μm double-poly nwell process. Figure 2(a) shows the noise due to the input device vs. device width for L=2 μm PMOS at 1 μsec peaking time, 5 mA drain current, and $C_{in}$=100pF. The optimum device width is about 40,000 μm; we chose W=10,000 μm since the increase in noise is negligible. Once the optimum width is chosen, the noise can be reduced by increasing the bias current. As shown in Fig. 2(b), the ENC decreases only as $Id^{-1/4}$.

Important secondary noise sources are the current source for the preamp input device and the input stage of the shaper. The schematics of the IPC and CSC preamps are shown in Fig. 3(a) and (b) respectively. Figure 4 shows a schematic of the shaper, which is based on a design by Chang[1]. The device sizes are given in Table 2 for IPC and CSC, which were chosen to give a peaking time of 25 and 1000 nsec, respectively. In this shaper design, the time constant of the low-pass sections can be adjusted electronically by varying the bias current.

## III. Results

Fig. 5(a) shows the ENC of the IPC preamp as a function of peaking time for various input capacitances. The measurement was made using an external $CR^2$-$RC^4$ shaper with programmable time constant. The simulated values, shown as light lines, are within 30% of the measured data over 3 decades of peaking time.

Fig. 5(b) shows impulse response waveforms of the IPC preamp and shaper. Noise measured at the shaper output was significantly effected by excess second-stage noise contributed by the shaper.Fig. 6(a) shows linearity measurements of the IPC preamp for positive and negative input polarity. In Fig. 6(b) we show the response of 7 channels overlaid on the same plot. The gain of 30 preamp channels measured from 4 chips from the same run was 0.984 +/- 3.1%.

Fig. 7 presents the output waveform of the CSC preamp/slow shaper/track-and-hold circuit, showing the effect of delaying the hold signal relative to the input. On this IC, the measured noise was 1900 $e^-$ + 11 e-/pF•Cin. Again, second-stage noise contributed significantly to the ENC, as well as excess parallel noise from the feedback resistive FET in the charge-sensitive stage.

The IPC preamps have been tested with a small cathode strip chamber. In this measurement, position interpolation is performed using 1usec shapers and an analog centroid finding system [2]. A collimated beam of X-rays is incident above the center of one cathode strip, and the position is measured repeatedly while the gas gain of the chamber is varied. The resulting resolution is plotted as small filled diamond symbols in Fig. 8. The ordinate is the total avalanche charge on the anode in a 1 μsec collection time (the cathode strips collect about 40% of this charge). Above 0.1 pC the position resolution is limited by delta rays and other physical processes in the gas to about 50 μm. Below 0.1 pC the position resolution is degraded by electronics noise and becomes inversely proportional to $Q_{anode}$. For comparison, the same chamber was instrumented with hybrid charge-sensitive preamplifiers having good low-noise JFET front end devices. The results, shown as open triangles, indicate that the CMOS device makes no significant contribution to the position resolution until the input charge falls below about 0.1 pC.

The remaining curves in Fig. 8 are obtained by injecting charge directly into the cathode strips through capacitors in a 1:3:1 ratio to simulate the charge pattern produced by anode avalanche. Using the same centroid-finding technique, we see the $1/Q_{anode}$ relationship continuing over a wider range of charge. In the electronic-noise dominated regime below 0.08 pC, we can estimate the ENC from the measured position resolution using: $\sigma_x / x_{RO} = \sqrt{3}(\sigma_Q / Q_{anode}) = \sqrt{3}(\sigma_Q / 0.4 Q_{cathode})$

We find ENC ~ 1100 $e^-$ for CMOS compared to 720 $e^-$ for the JFET hybrid circuit. At 1 μsec shaping time CMOS suffers from 1/f noise while the JFET remains below its 1/f noise corner time constant.

## IV. Comparison with other Monolithic Charge Sensitive Preamps

In Fig. 9 we plot the noise slope ($dENC/dC_{in}$) as a function of peaking time for various preamplifiers reported in the literature [3-7]. The noise slope provides a better basis for comparison than the total ENC because it depends only on preamplifier characteristics. The diagonal lines represent the contours of equal equivalent input noise expressed as an equivalent noise resistance $R_n$. The octagons surrounding each point have a radius proportional to the square root of the power dissipation; hence the desirable preamplifier characteristics lie to the lower left of the plot with a small octagon. Note that most CMOS preamps have $R_n$ >300Ω, bipolar circuits lie between 10-100Ω for $t_p$ < 30 nsec, and hybrid and JFET circuits can reach 10Ω $R_n$ with higher power. The only CMOS ASICs with $R_n$ < 100Ω are the CERN ICON [7], the ASIC from the University of Leuven [1], and the IPC preamp reported here. The ICON is a current sensitive design which cannot be used at shaping times longer than about 20 nsec because of parallel noise. The Leuven design achieves low $R_n$ by using a very large input device (30,000/3 um) and high power, which permits only a single channel per chip.

## V. Future Plans

A version of the IPC preamp with integrated 25 nsec shaper has been designed in the Harris AVLSI-RA radiation hard process. We plan to implement integrated calibration capacitors and switches in future ASICs as shown in Fig. 1. In the CSC chip, configuration switches will be provided to allow the user to program gain and peaking time, and to select between multiplexed and parallel output of the amplitude readout channel. We will test the current prototypes for ESD susceptibility and will implement im-

proved protection against chamber discharge. The preamp feedback resistance will be adjustable to control the parallel noise, and pole-zero networks will be used to cancel the preamp feedback pole and the long $1/(1+t/t_0)$ tail of the gas detector signal.

## VI. Summary and Conclusions

Two custom ASICs for GEM cathode pad/strip chambers are in development. In test results on prototypes we obtained 340 + 33 $e^-$/pF for an NMOS-input preamp at 30 nsec shaping time, and noise performance at other peaking times that agrees with simulated values. Both preamps have less than 1% nonlinearity up to above 500 fC input charge. Power dissipation is 29 mW/channel in an 8-channel ASIC. The PMOS-input preamp has been tested with an integrated 750 nsec semiGaussian shaper and track-and-hold. The noise of the combined circuit is 1900 + 11 e-/pF. In future developments we will integrate additional functionality, reduce second-stage noise, and investigate other processes for improved radiation tolerance and noise performance.

## References


1. Chang, Z.Y. and Sansen, W. , Low Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies, Chapt. 5, Kluwer, 1991
2. V. Radeka, R. Boie, “Centroid Finding Method for Position-Sensitive Detectors”, Nucl. Instr. Methods 178 (1980), 543-554
3. E. Nygard et. al., “CMOS low noise amplifier for microstrip readout, design and results” , Nucl. Instr. Methods A301 (1991), 506-516
4. F. Anghinolfi et. al., “Study of Analogue Front-End Electronics for SUpercollider Experiments”, presented at the ECFA Large Collider Workshop 4-9 October 1990, Aachen, Germany
5. P. Jarron, M. Goyot, “A Fast Current Sensitive Preamplifier (MSD2) for the Silicon Microstrip Detector”, Nucl. Instr. Methods 226 (1989), 156-163
6. F. Newcomer et. al.., “A Fast Monolithic Preamp and SHaper for High Rate Gas Tracking Detectors”, presented at the IEEE Nucl. Science Symposium, Oct. 1990, Philadelphia PA
7. F. Anghinolfi et. al.., “ICON, a Current Mode Preamplifier In CMOS Technology for Use With High-Rate Particle Detectors”, presented at the IEEE Nucl. Science Symposium, 5-9 November 1991, Santa Fe
8. S. Tedja et. al., “New Preamplifier and Analog Memory Designs for Silicon Strip Readout”, private communication
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## IPC preamp/shaper

1. Input capacitance (pad + readout line): 10 - 50 pF
2. Most Probable Qpad: ~ 30 fC (200,000 e-)
3. Rate: up to 200 kHz/pad
4. Noise: < 2000 $e^-$ [1000 desirable]
5. Voltage output: semiGaussian pulse 30 nsec peaking time
6. Charge-to-voltage gain: 10 mV/fC
7. Linear range: to 150 fC input charge
8. Radiation tolerance: to 2 Mrad, 2e14 n/cm2

## CSC cathode readout chip

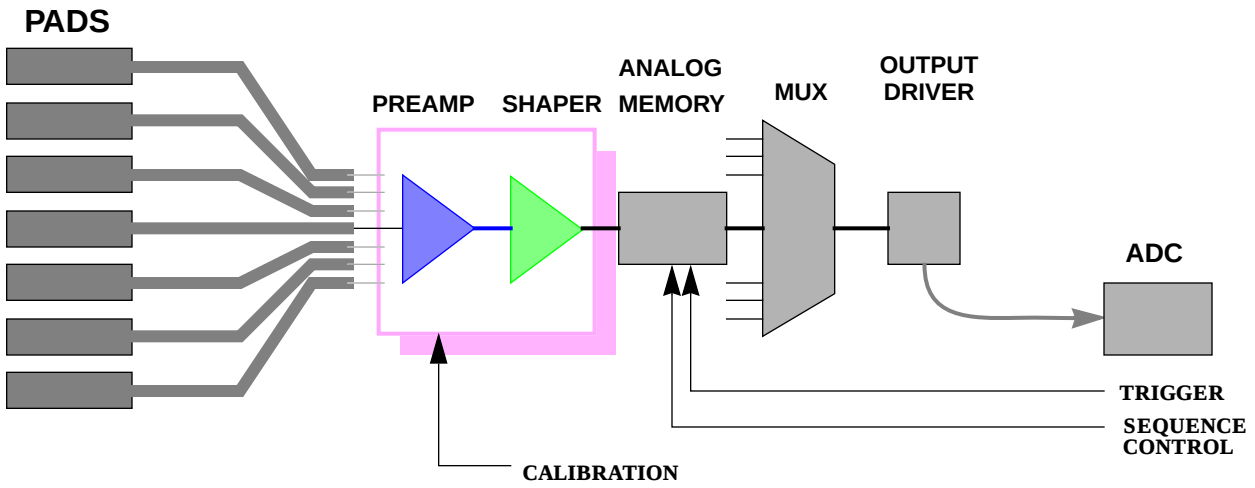
1. Strip capacitance: 50 - 150 pF
2. Most probable Qstrip: ~ 50 fC
3. Track rate: ~ 100 Hz/strip
4. Background rate: 5 kHz/strip (depends on neutron flux & detection efficiency)
5. Noise: < 2000 $e^-$
6. Gain: ~ 10 mV/fC
7. Linear range: to 150-250 fC
8. Outputs:
    a) Readout: 300 nsec semiGaussian through track/hold, analog mux
    b) Timing: 30 nsec semiGaussian, all channels output in parallel

**Table 1: Front End ASIC Design Requirements**

| Device | IPC shaper | CSC shaper |
|---|---|---|
| M1,M2 | 34/2 | 82/2 |
| M3,M4 | 8/2 | 52.5/21 |
| M5,M6 | 112/2 | 630/21 |
| M7,M8 | 30/2 | 24/3 |
| R1 | 5K | 3K |
| R2 | 50K | 50K |
| CL | 1p | 50p |

**Table 2: Shaper Device Sizes (see Fig. 4)**

## IPC Readout Chain




## CSC Readout Chain

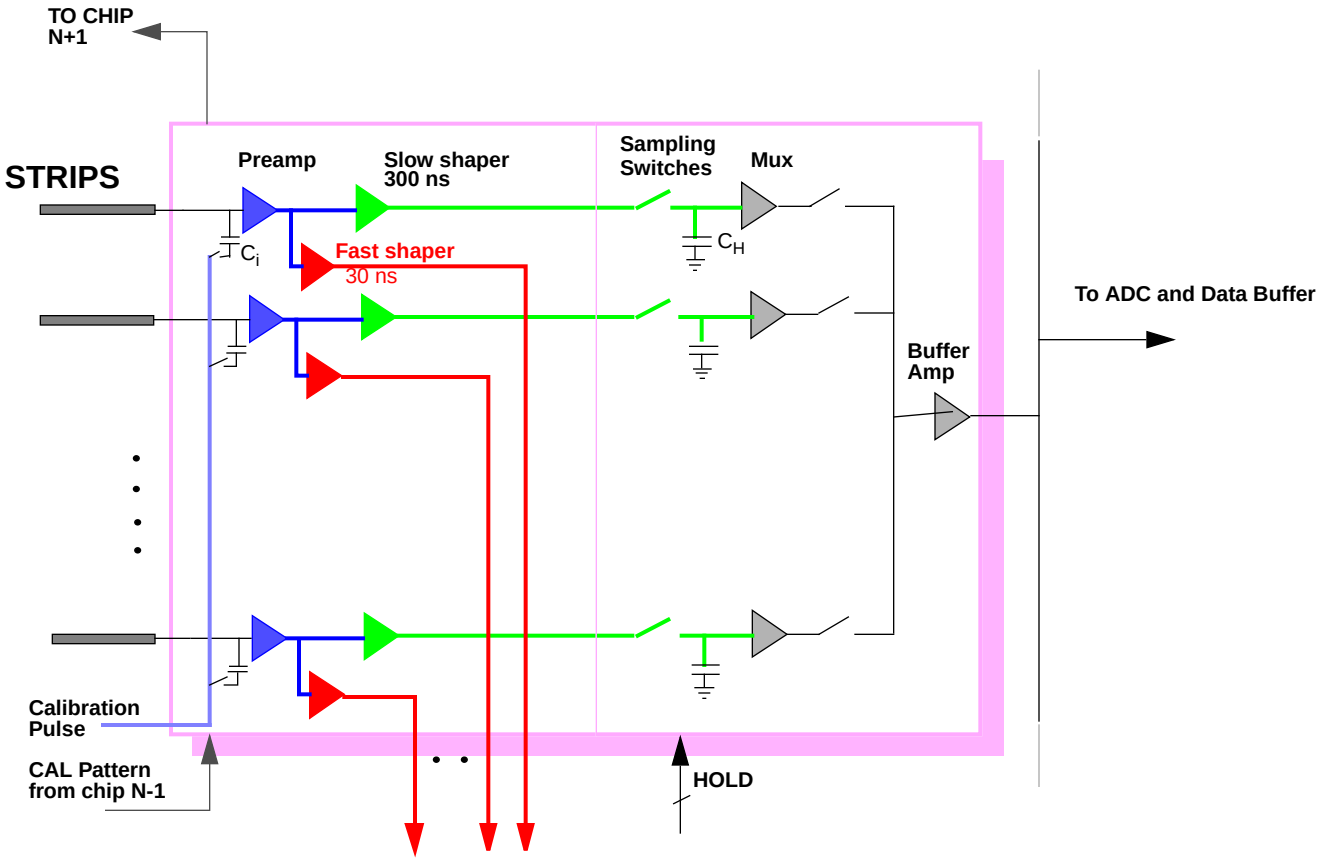



**Figure 1**

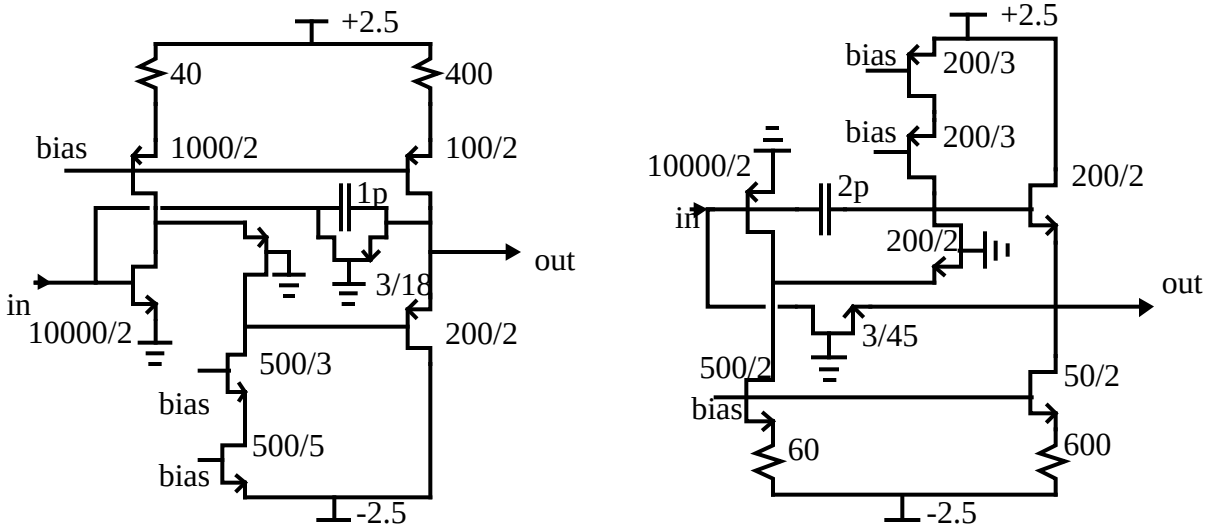



**Figure 3**

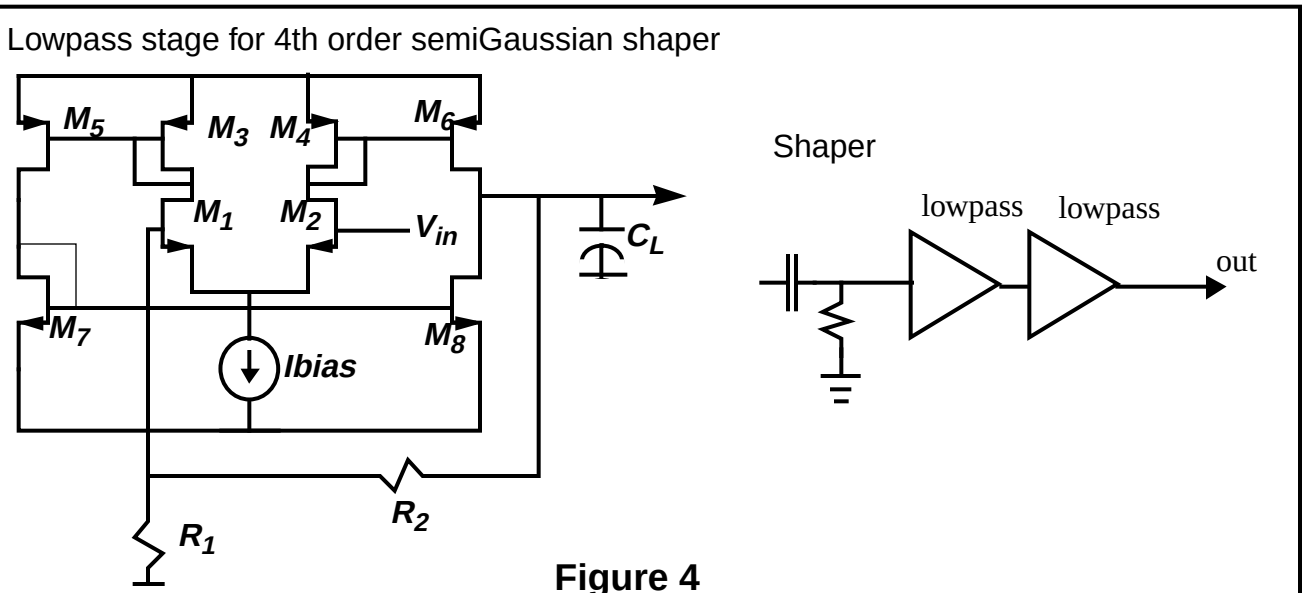
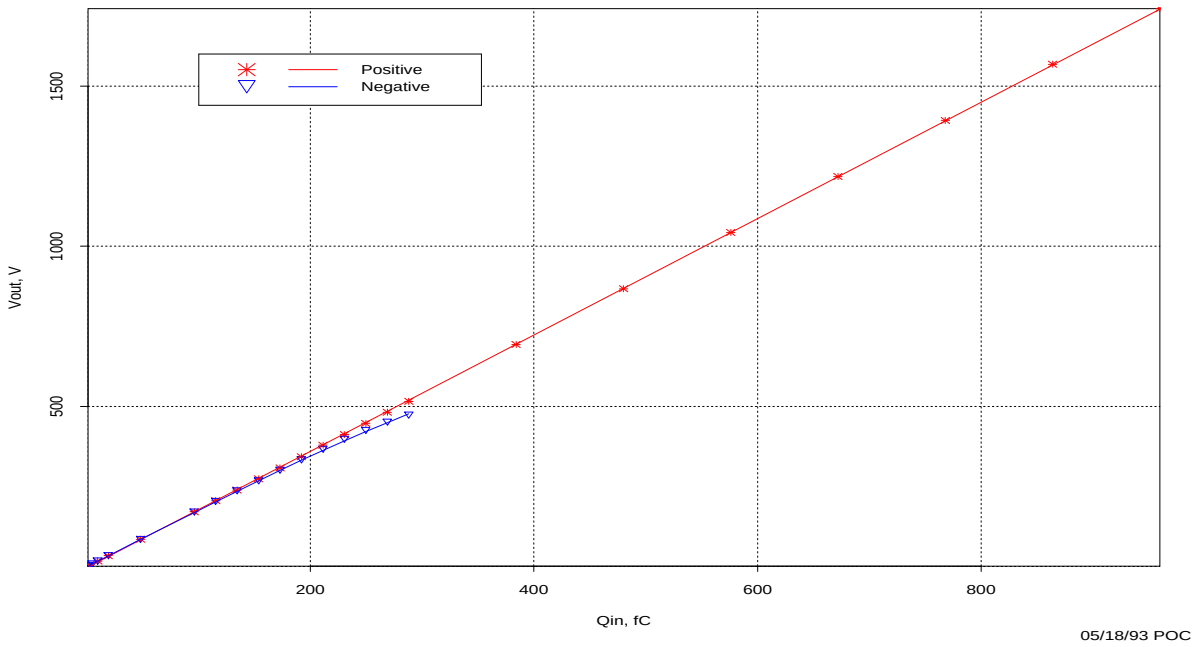



**Figure 4**

**Table 2**

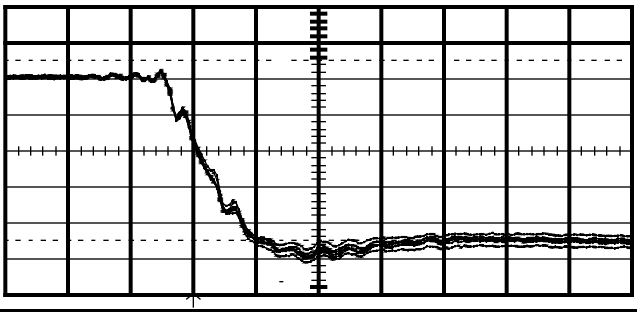
| Device | IPC shaper | CSC shaper |
|---|---|---|
| M1,M2 | 34/2 | 82/2 |
| M3,M4 | 8/2 | 52.5/21 |
| M5,M6 | 112/2 | 630/21 |
| M7,M8 | 30/2 | 24/3 |
| R1 | 5K | 3K |
| R2 | 50K | 50K |

Preamp_n Linearity




NMOS-input preamp: Qin=50mV through 1pF: 7 channels overlay

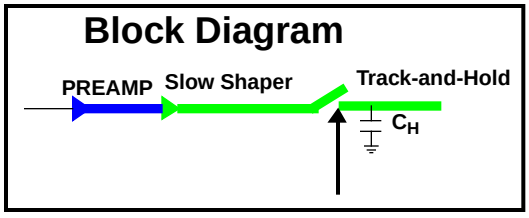
Gain: 0.984 mV/fC +/- 3.1% for 30 channels

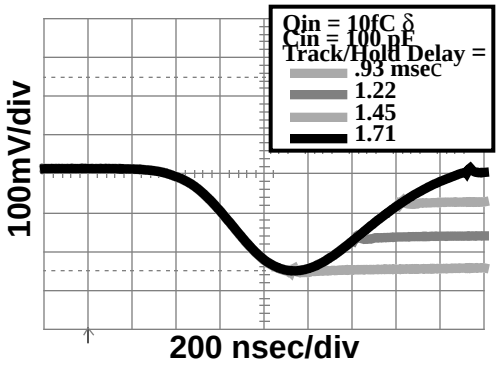


20 ns/div
10 mV/div

**Figure 6**

## Track and Hold Output Waveform




Noise: 1800 + 11.3 e-/pF
Linearity: to 250 fC Qin

**Figure 7**

## Position Resolution Measurement with Cathode Strip Chamber

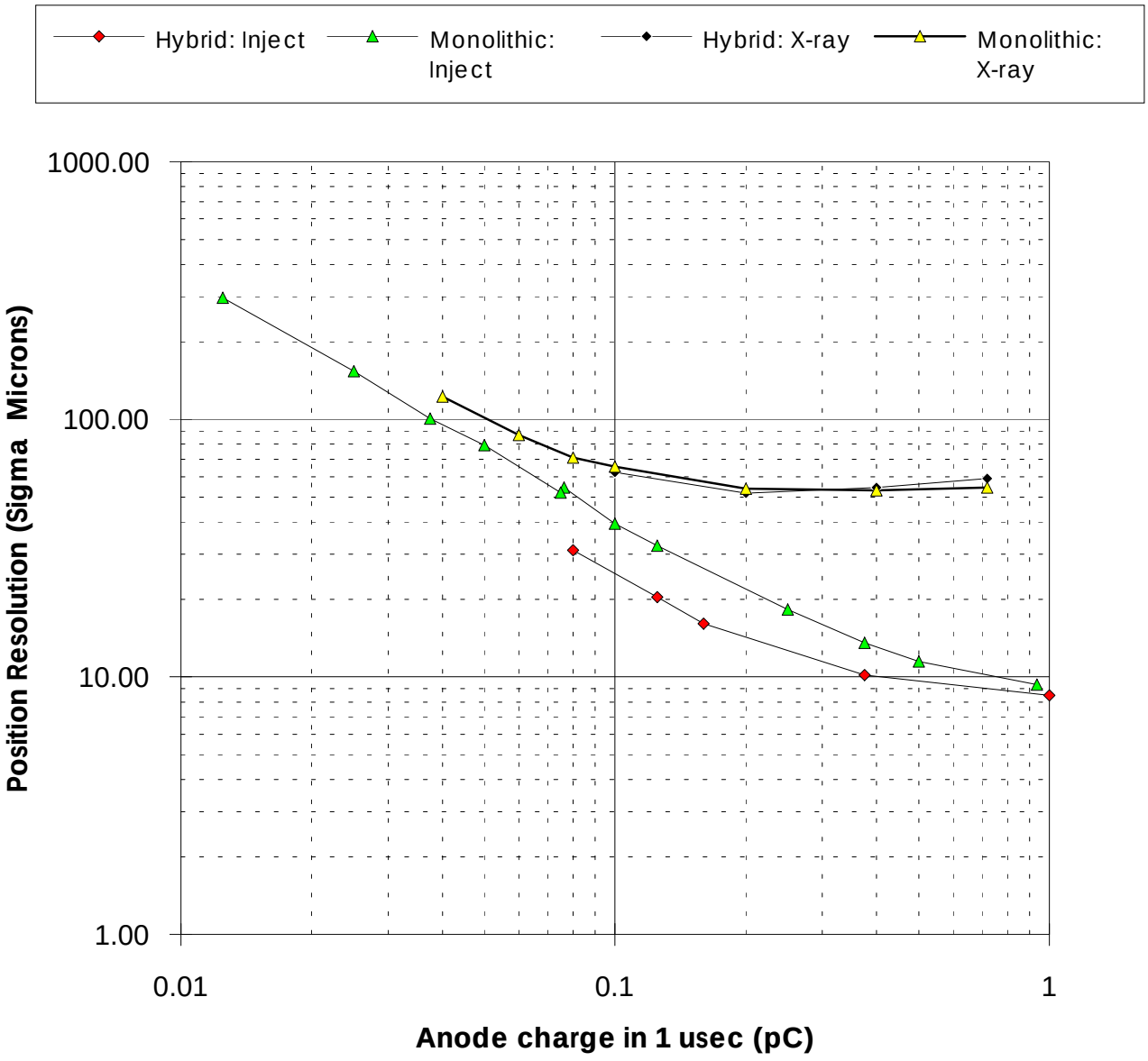



**Figure 8**

# Noise/Peaking Time/Power Comparison of Reported ASIC Preamplifiers

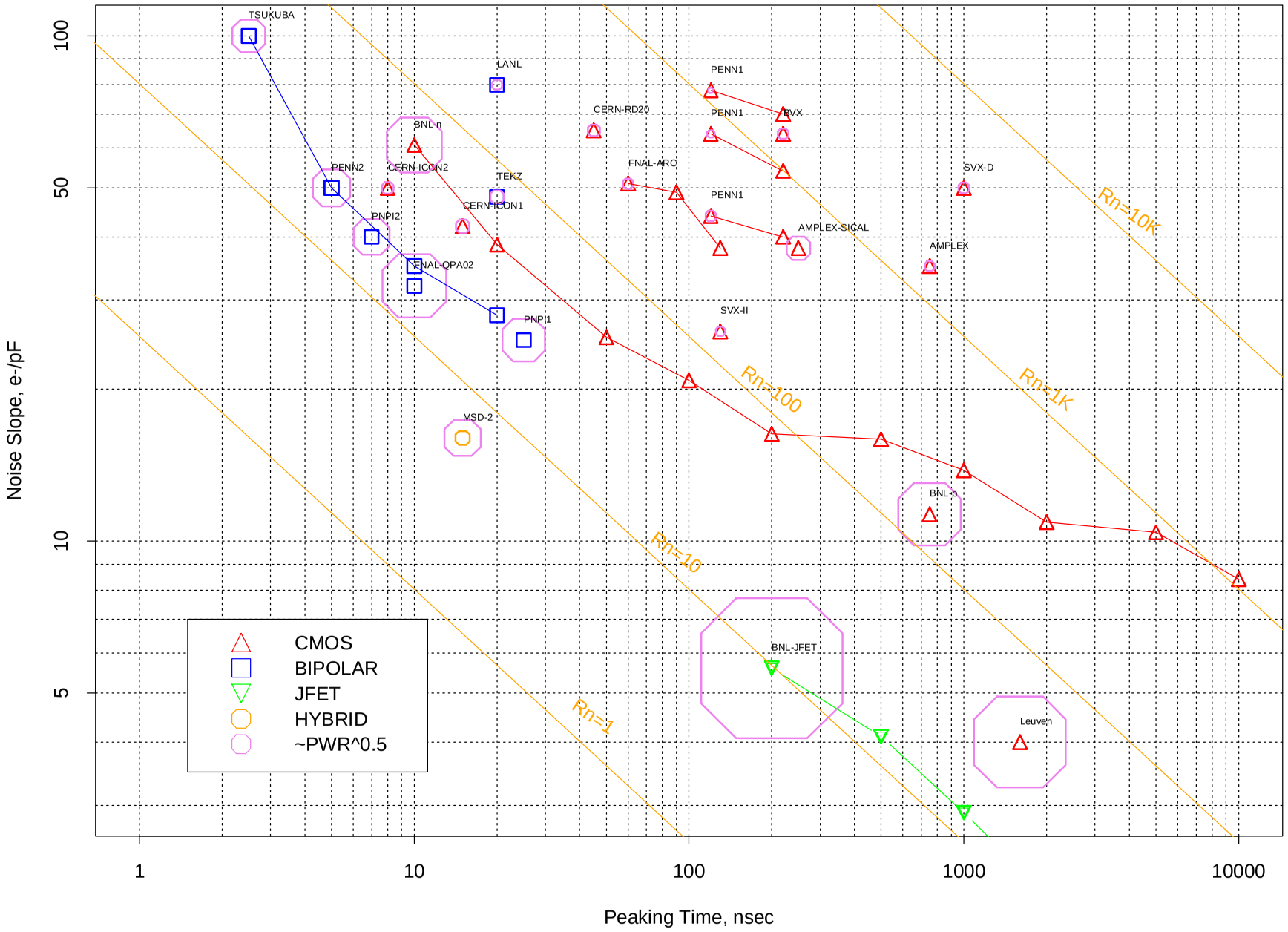



**Figure 9**

# Charge Sensitive Preamp: Optimization of Input Device

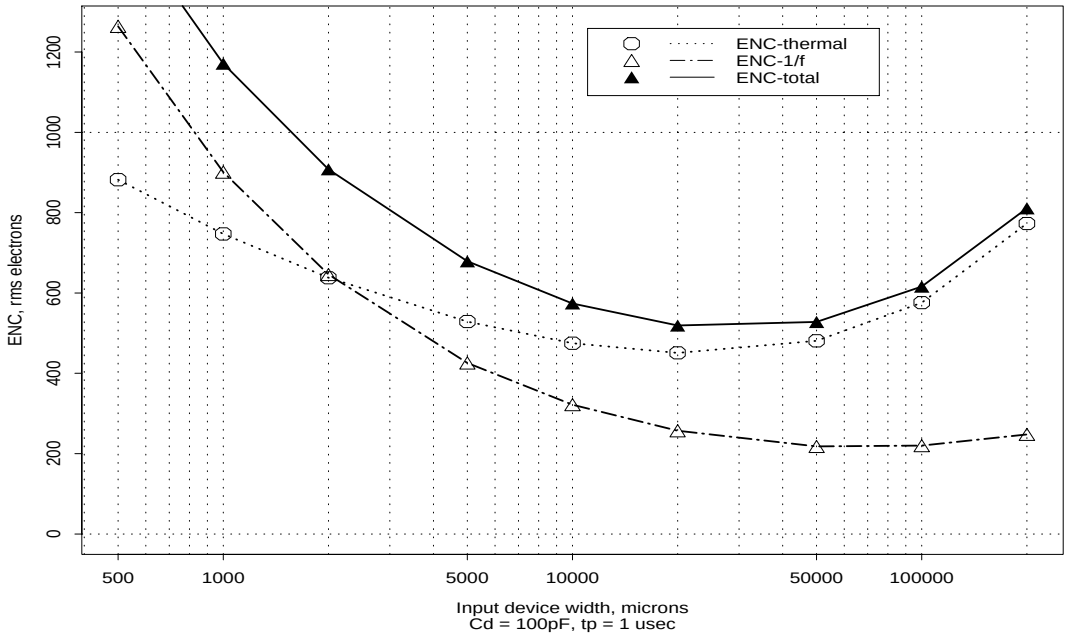
Equivalent input noise charge:

$$ENC^2 = a_1 \frac{C_T^2 e_n^2}{\tau_m} + a_2 i_n^2 \tau_m \qquad \textbf{(EQ 1)}$$

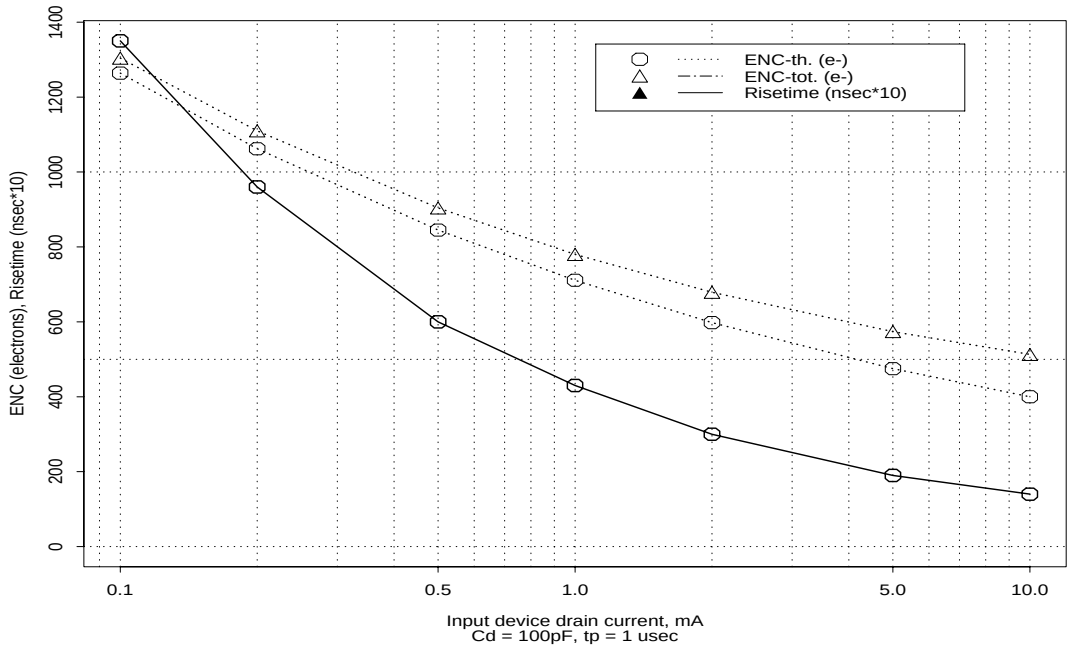
for MOS,

$$e_n^2 = 4kT\left(\frac{2\Gamma}{3g_m} + R_g\right) + a_3 \tau_m \frac{K_f}{C_{ox}^2 WL} \qquad \textbf{(EQ 2)}$$

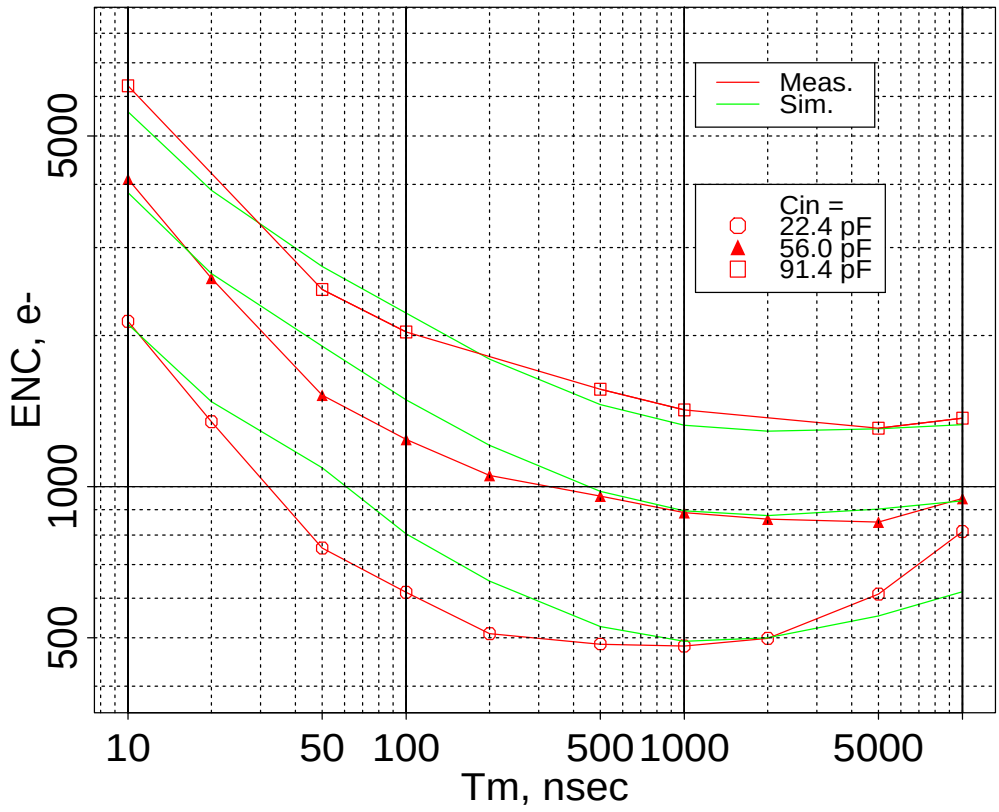
Optimization versus width:




Optimization versus drain current: **ENC ~ $I_d^{-1/4}$**



## ENC vs. Tm for CMOS Preamp
## with 10000/2 μm n-channel input device




## Preamp and Shaper Waveforms: 20 nsec/div